Design and Generation of High-Performance Transceivers

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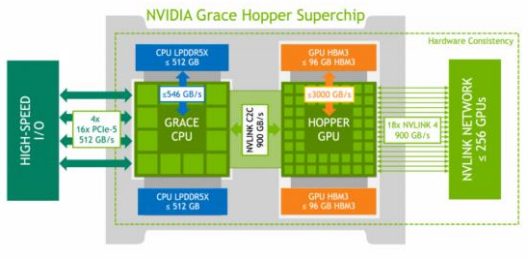
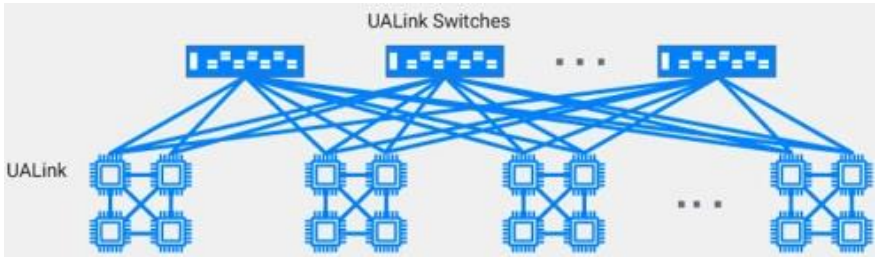
Motivation

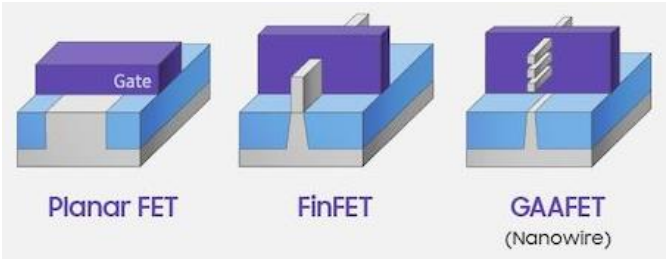
- **Bandwidth Scale-Up:** In the AI era, high-performance transceivers are essential to handle massive data, requiring over **100 Gb/s per channel**

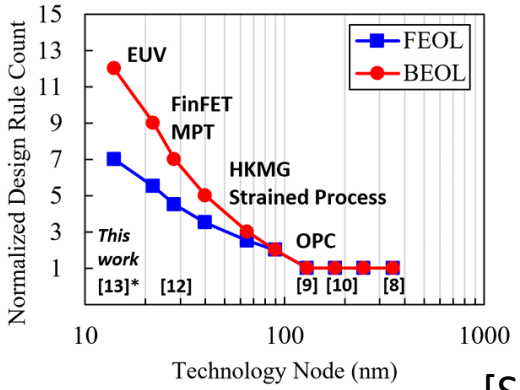




[NVIDIA, Synopsys]

- **Design Complexity:** Designing and fabricating these circuits in nanometer technologies require significant time and effort

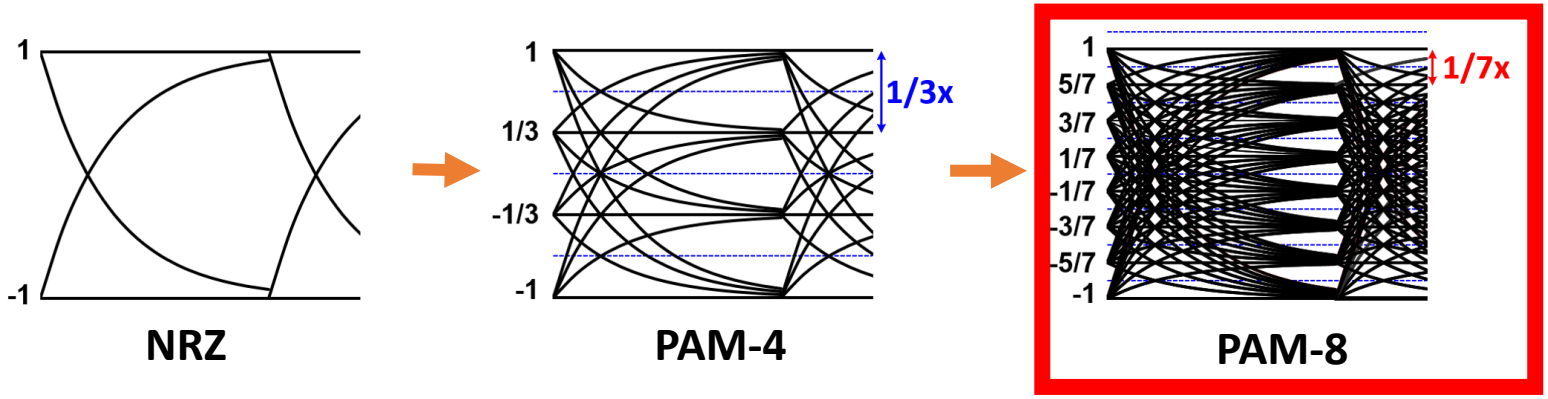




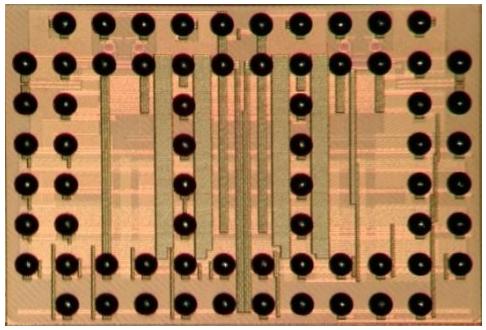
[Samsung, J. Han]

High-Bandwidth Solution: PAM-X Transmission

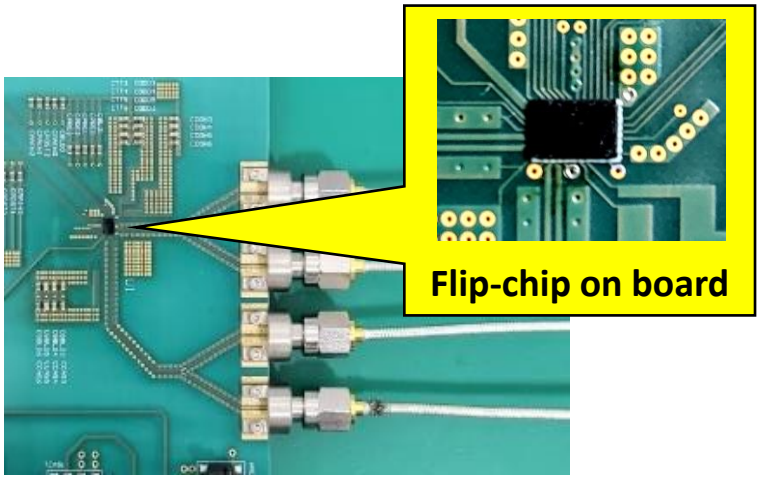
- Increase the number of transmitted bits per symbol



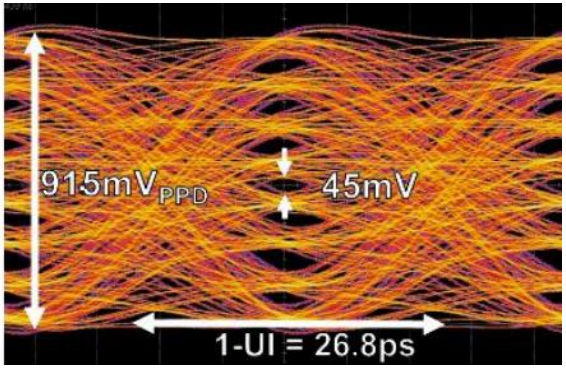
PAM Signal Evolutions



Chip Micrograph



Measurement Setup

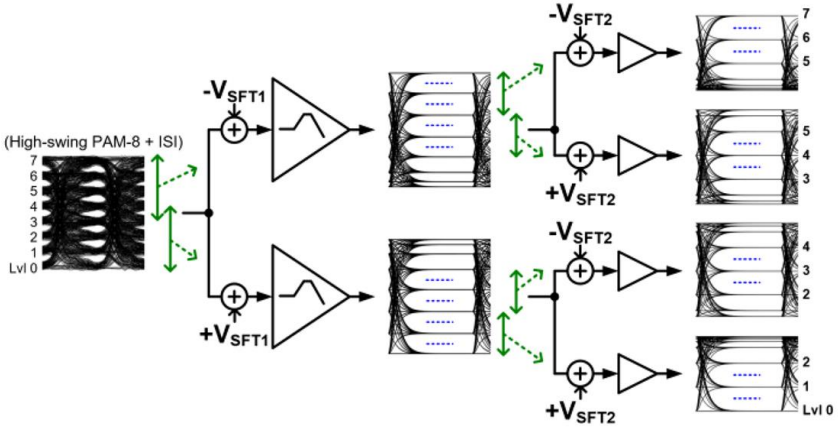


112Gb/s PAM8 Eye Diagram

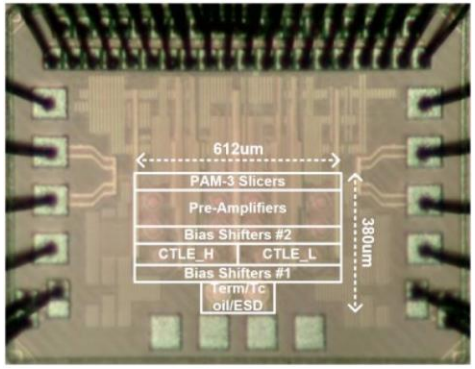
[J. Han, ISSCC 2023]

High-Bandwidth Solution: PAM-X Reception

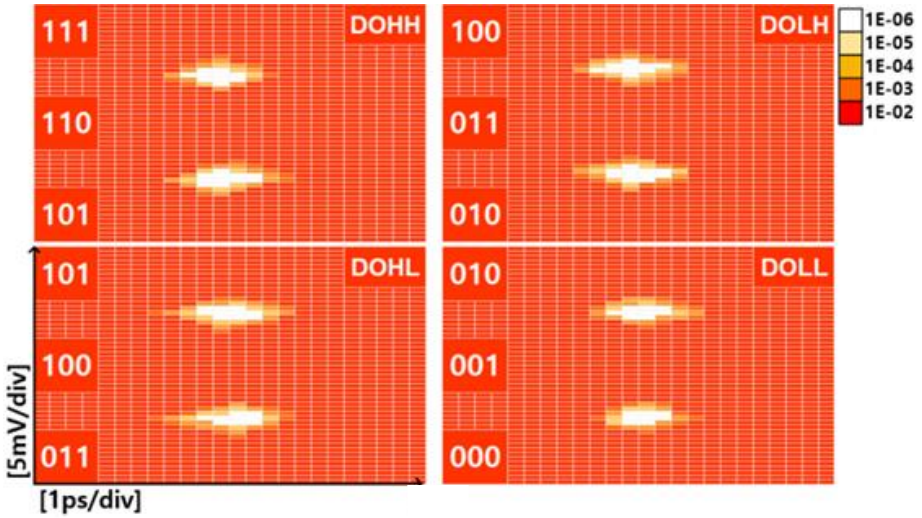
- A multi-path receive chain ensures high-fidelity recovery of PAM-8 signals, demonstrating **the highest PAM-8 mixed-signal data rate** ever reported



Receiver Architecture



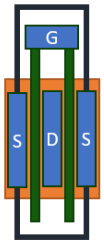
Chip Micrograph



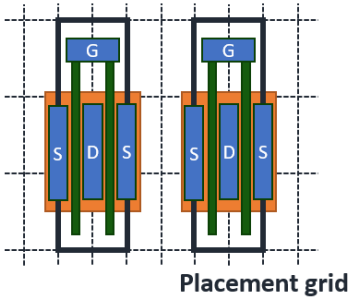
Measured Eye Diagrams at 103Gb/s

High Productivity Solution: Design Automation (1)

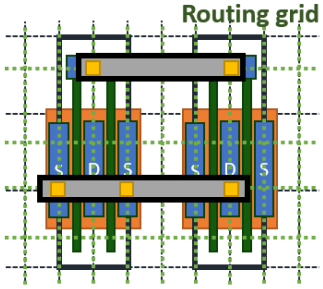
- Our framework, **LAYGO**, automates layout generation using templates and grids



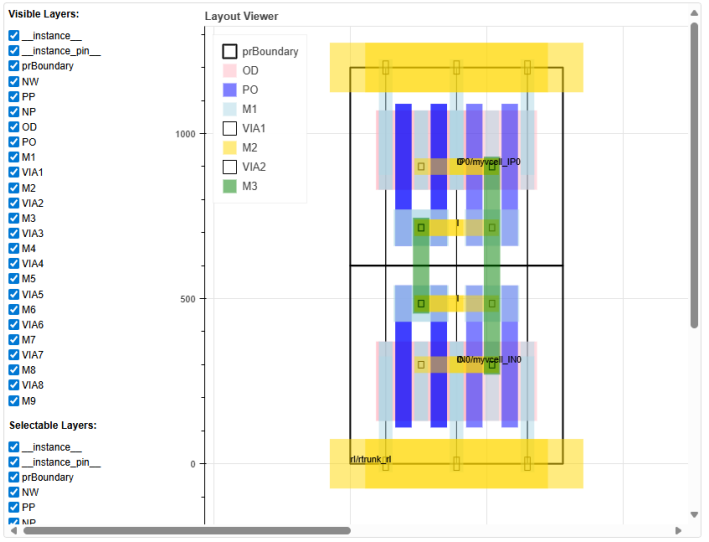
Templates



On-grid placement



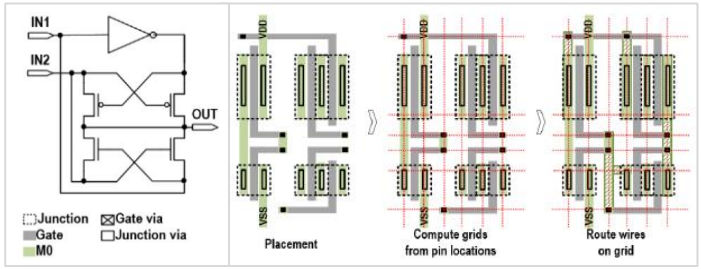
On-grid routing

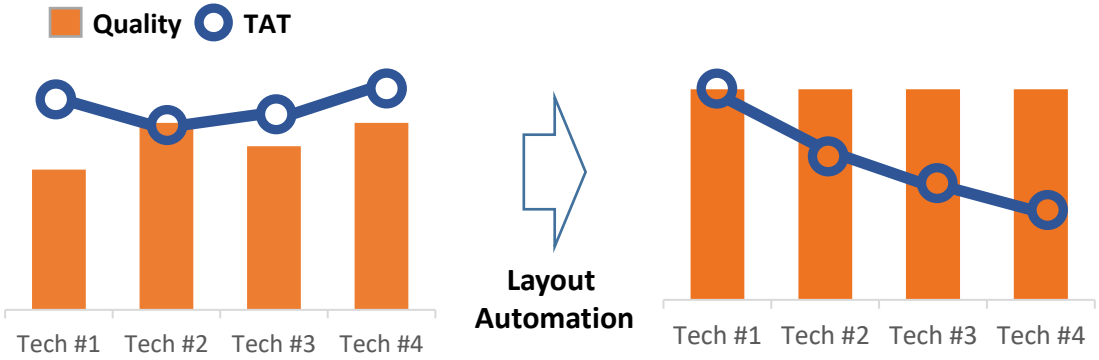


A temporary website is open, please try! - **http://laygo.hanyang.ac.kr**

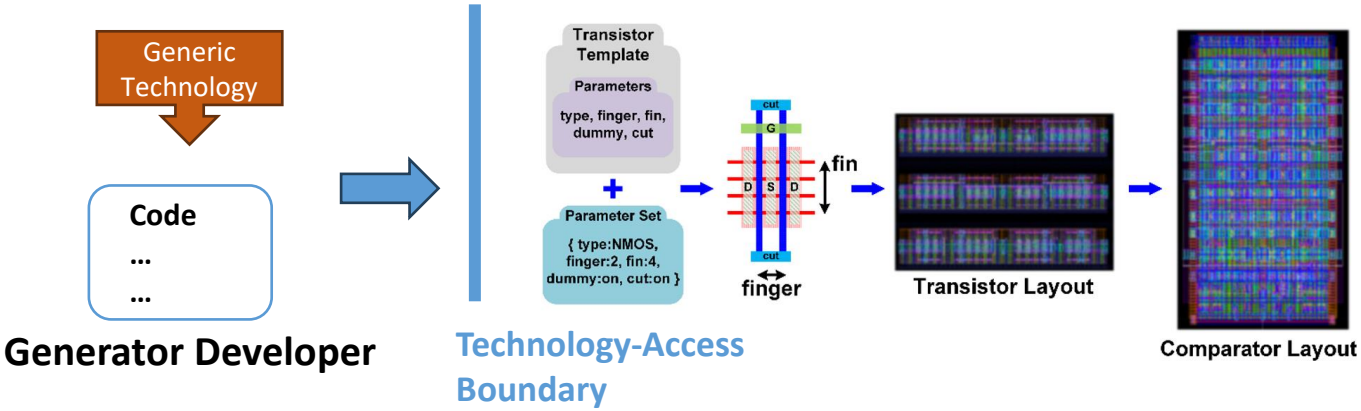
High Productivity Solution: Design Automation (2)

- Applied to sub-7nm FinFET, DRAM, and CIS, over **5x productivity improvement** is **proven**
- We're now integrating AI and LLMs—**stay tuned!**





[SK Hynix]



[Ramschip]

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